WE CLAIM:

1. A method of forming a magnetic memory cell, comprising:

providing a first conductive layer as a blanket layer;

providing a barrier layer as a blanket layer over the first conductive layer;

providing a second conductive layer as a blanket layer over the barrier layer;

providing a hard mask over the second conductive layer, wherein the hard mask defines the region in which the magnetic memory cell is formed;

etching the second conductive layer to form an upper portion of the magnetic memory cell;

forming a spacer around the upper portion of the magnetic memory cell;

etching the barrier layer and the first conductive layer to form a lower portion of the magnetic memory cell, wherein conductive particles of the first conductive layer may be thrown up along a sidewall of the magnetic memory cell as byproducts of the etching of the first conductive layer; and

oxidizing the magnetic memory cell, thereby transforming the conductive particles into nonconductive particles.

2. The method of Claim 1, further comprising oxidizing the outer portions of the second conductive layer after it is etched to form the upper portion of the magnetic memory cell.

3. The method of Claim 2, wherein oxidizing the outer portions of the second conductive layer comprises subjecting the outer portions of the second conductive layer to plasma oxidation.

4. The method of Claim 2, wherein oxidizing the outer portions of the second conductive layer comprises using O_3 as an oxidant, at a flow rate within the range of about 100 sccm to about 500 sccm.

5. The method of Claim 1, wherein the first conductive layer comprises a first sublayer comprising tantalum, a second sublayer comprising nickel-iron, a third sublayer comprising magnesium oxide, irridium-manganese, platinum-manganese or nickel-manganese, and a fourth sublayer comprising nickel-iron or cobalt-iron.

6. The method of Claim 5, wherein the first conductive layer has a thickness within the range of about 1 nm to about 30 nm.

7. The method of Claim 1, wherein the barrier layer comprises aluminum oxide and has a thickness within the range of about 0.5 nm to about 3 nm.

8. The method of Claim 1, wherein the second conductive layer comprises a first sublayer comprising tantalum, a second sublayer comprising tungsten nitride, and a third sublayer comprising nickel-iron, cobalt or copper.

9. The method of Claim 8, wherein the second conductive layer has a thickness within the range of about 1 nm to about 30 nm

10. The method of Claim 1, wherein the hard mask comprises a material selected from the group consisting of silicon nitride, silicon oxynitride, and silicon carbide.

11. The method of Claim 10, wherein the hard mask has a thickness within the range of about 500 Å to about 2000 Å.

12. The method of Claim 1, wherein etching the second conductive layer comprises ion milling, reactive ion etching, or chemical etching.

13. The method of Claim 12, wherein etching the second conductive layer comprises using CO_2-NH_3 or CO-NH_3 as an etchant.

14. The method of Claim 1, wherein forming a spacer comprises:

depositing a layer of nonconductive material as a blanket layer over the upper portion of the memory cell; and

anisotropically etching the layer of nonconductive material such that the horizontal portions of the layer are preferentially removed relative to the vertical portions of the layer.

15. The method of Claim 14, wherein the layer of nonconductive material has a thickness within the range of about 5 nm to about 100 nm.

16. The method of Claim 14, wherein anisotropically etching the layer of nonconductive material comprises ion milling or reactive ion etching.

17. The method of Claim 16, wherein the nonconductive material comprises silicon nitride and anisotropically etching the layer of nonconductive material comprises using a fluorocarbon as an etchant.

18. The method of Claim 16, wherein the nonconductive material comprises diamond-like carbon and anisotropically etching the layer of nonconductive material comprises using oxygen-based plasma as an etchant.

19. The method of Claim 16, wherein the nonconductive material comprises silicon carbide and anisotropically etching the layer of nonconductive material comprises using a fluorocarbon as an etchant.

20. The method of Claim 1, wherein the spacer comprises a low k electrical insulator having a k value of less than about 3.5.

21. The method of Claim 20, wherein the spacer comprises a material selected from the group consisting of silicon nitride, diamond-like carbon, silicon carbide, silicon oxide, and aluminum oxide.

22. The method of Claim 1, wherein etching the barrier layer and the first conductive layer comprises ion milling, reactive ion etching, or chemical etching.

23. The method of Claim 22, wherein etching the barrier layer and the first conductive layer comprises using CO_2-NH_3 or CO-NH_3 as an etchant.

24. The method of Claim 1, wherein oxidizing the memory cell comprises subjecting the memory cell to plasma oxidation.

25. The method of Claim 1, wherein oxidizing the memory cell comprises using O_3 as an oxidant, at a flow rate within the range of about 100 sccm to about 500 sccm.

26. The method of Claim 1, wherein the memory cell comprises a tunneling magnetoresistance (TMR) memory cell.

27. A method of forming a magnetic memory cell, comprising:

providing a first conductive layer, a barrier layer, and a second conductive layer as blanket layers;

providing a hard mask over the second conductive layer, wherein the hard mask defines the region in which the magnetic memory cell is formed;

etching the second conductive layer and the barrier layer to form an upper portion of the magnetic memory cell;

partially oxidizing the first conductive layer such that at least a portion of the first conductive layer is transformed into an insulating material;

at least partially etching the portion of the first conductive layer that was transformed into an insulating material during the partial oxidizing step; and

repeating the partial oxidizing and partial etching steps until the first conductive layer forms a lower portion of the magnetic memory cell.

28. The method of Claim 27, wherein the first conductive layer comprises a first sublayer comprising tantalum, a second sublayer comprising nickel-iron, a third sublayer comprising magnesium oxide, irridium-manganese, platinum-manganese or nickel-manganese, and a fourth sublayer comprising nickel-iron or cobalt-iron.

29. The method of Claim 28, wherein the first conductive layer has a thickness within the range of about 1 nm to about 30 nm.

30. The method of Claim 27, wherein the barrier layer comprises aluminum oxide and has a thickness within the range of about 0.5 nm to about 3 nm.

31. The method of Claim 27, wherein the second conductive layer comprises a first sublayer comprising tantalum, a second sublayer comprising tungsten nitride, and a third sublayer comprising nickel-iron, cobalt or copper.

32. The method of Claim 31, wherein the second conductive layer has a thickness within the range of about 1 nm to about 30 nm

33. The method of Claim 27, wherein the hard mask comprises a material selected from the group consisting of silicon nitride, silicon oxynitride, and silicon carbide.

34. The method of Claim 33, wherein the hard mask has a thickness within the range of about 500 Å to about 2000 Å.

35. The method of Claim 27, wherein etching the second conductive layer and the barrier layer comprises ion milling, reactive ion etching, or chemical etching.

36. The method of Claim 35, wherein etching the second conductive layer and the barrier layer comprises using CO_2-NH_3 or CO-NH_3 as an etchant.

37. The method of Claim 27, wherein partially oxidizing the first conductive layer comprises a plasma oxidation process.

38. The method of Claim 27, wherein partially oxidizing the first conductive layer comprises using O_3 as an oxidant, at a flow rate within the range of about 100 sccm to about 500 sccm.

39. The method of Claim 27, wherein partially etching the first conductive layer comprises ion milling, reactive ion etching, or chemical etching.

40. The method of Claim 39, wherein partially etching the first conductive layer comprises using CO_2-NH_3 or CO-NH_3 as an etchant.

41. The method of Claim 27, wherein the memory cell comprises a tunneling magnetoresistance (TMR) memory cell.

42. A magnetic memory cell, comprising:

a lower layer comprising a first conductive material;

a middle layer comprising an insulating material;

an upper layer comprising a second conductive material; and

a nonconductive layer comprising an oxide of the first conductive material, wherein the nonconductive layer is coated along a sidewall of the magnetic memory cell such that it can be in contact with both the upper and lower layers.

43. The magnetic memory cell of Claim 42, wherein the nonconductive layer comprises a continuous layer of material.

44. The magnetic memory cell of Claim 42, wherein the nonconductive layer comprises a discontinuous layer of material.

45. The magnetic memory cell of Claim 42, wherein outer portions of the upper layer comprise an oxide of the second conductive material.

46. The magnetic memory cell of Claim 42, wherein the lower layer comprises a first sublayer comprising tantalum, a second sublayer comprising nickel-iron, a third sublayer comprising magnesium oxide, irridium-manganese, platinum-manganese or nickel-manganese, and a fourth sublayer comprising nickel-iron or cobalt-iron.

47. The magnetic memory cell of Claim 46, wherein the lower layer has a thickness within the range of about 1 nm to about 30 nm.

48. The magnetic memory cell of Claim 42, wherein the middle layer comprises aluminum oxide and has a thickness within the range of about 0.5 nm to about 3 nm.

49. The magnetic memory cell of Claim 42, wherein the second conductive layer comprises a first sublayer comprising tantalum, a second sublayer comprising tungsten nitride, and a third sublayer comprising nickel-iron, cobalt or copper.

50. The magnetic memory cell of Claim 49, wherein the second conductive layer has a thickness within the range of about 1 nm to about 30 nm

51. The magnetic memory cell of Claim 42, wherein the upper layer is surrounded by a spacer.

52. The magnetic memory cell of Claim 51, wherein the spacer has a thickness within the range of about 5 nm to about 100 nm.

53. The magnetic memory cell of Claim 51, wherein the spacer comprises a low k electrical insulator having a k value of less than about 3.5.

54. The magnetic memory cell of Claim 53, wherein the spacer comprises silicon nitride, diamond-like carbon, silicon carbide, silicon oxide, or aluminum oxide.

55. The magnetic memory cell of Claim 51, wherein the magnetic memory cell comprises a tunneling magnetoresistance (TMR) memory cell.

56. The magnetic memory cell of Claim 51, wherein the magnetic memory cell comprises a giant magnetoresistance (GMR) memory cell.

57. A magnetic memory cell, comprising:

a lower layer comprising a first conductive material;

a middle layer comprising an insulating material;

an upper layer comprising a second conductive material surrounded by a spacer material; and

at least one sidewall coated with oxidized particles of the first conductive material.